

REFERENCES:

[1] A.A. Abdidi, "Direct-Conversion Radio Transceivers for Digital communications", *IEEE Journal of Solid-State Circuit*, Vol.30, No.12, pp 1399-1410, December 1995

[2] P.M. Street, R. McLindra, S. Hahn, A. Schuur, E. Riou, "Zero-IF Single Chip Transceiver for Up-to Mbps QPSK 802.11b Wireless LAN", *IEEE International Solid State Circuits Conference Digest of Technical Papers*, Feb.2001, pp.204-205

Direct-Conversion Radio Transceivers for Digital Communications

Asad A. Abidi, *Senior Member, IEEE*

Abstract-Direct-conversion is an alternative wireless receiver architecture to the well-established superheterodyne, particularly for highly integrated, low-power terminals. Its fundamental advantage is that the received signal is amplified and filtered at baseband rather than at some high intermediate frequency. This means lower current drain in the amplifiers and active filters and a simpler task of image-rejection. There is considerable interest to use it in digital cellular telephones and miniature radio messaging systems. This paper briefly covers case studies in the use of direct-conversion receivers and transmitters and summarizes some of the key problems in their implementations. Solutions to these problems arise not only from more appropriate circuit design but also from exploiting system characteristics, such as the modulation format in the system. Baseband digital signal processing must be coupled to the analog front-end to make direct-conversion transceivers a practical reality.

I. INTRODUCTION

THE CURRENT interest in portable wireless communications devices is prompting research into new IC technologies, circuit configurations and transceiver architectures. Low-power miniature radio transceivers are sought to communicate digital data in cellular telephones, wireless networks, and radio messaging systems. While transistor technology *scaling* and *improved circuit techniques* will contribute evolutionary advances towards this goal, *architectural innovations* in the transceiver may lead to revolutionary improvements [1]. It is in this context that there is a resurgence of interest in direct-conversion.

The superheterodyne receiver, which Armstrong introduced in 1918 [2], is generally thought to be the receiver of choice owing to its high selectivity and sensitivity. Something like 98% of radio receivers use this architecture. In a superheterodyne receiver, the input signal is first amplified at RF in a tuned stage, then converted by an offset-frequency local oscillator to a lower intermediate frequency (IF), and substantially amplified in a tuned IF "strip" containing highly-selective passive bandpass filters. The role of the various filters is illustrated by the typical frequency plan of a superheterodyne receiver (Fig. 1). The IF must be sufficiently high so that the *image channel* lies in the stopband of the RF preselection filter or the antenna, otherwise the IF filter will pass this channel unattenuated in its own image passband. These considerations determine the familiar intermediate frequencies used in radio and TV receivers.

Manuscript received May 22, 1995; revised August 29, 1995.

The author is with the Electrical Engineering Department, University of California, Los Angeles, CA 90095 USA,
IEEE Log Number 9415818.

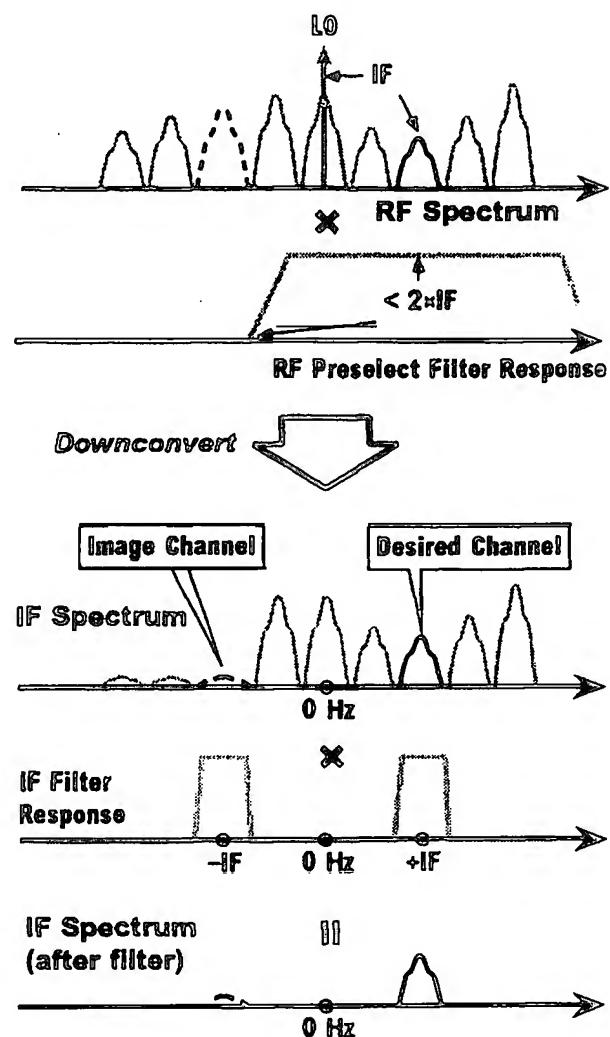


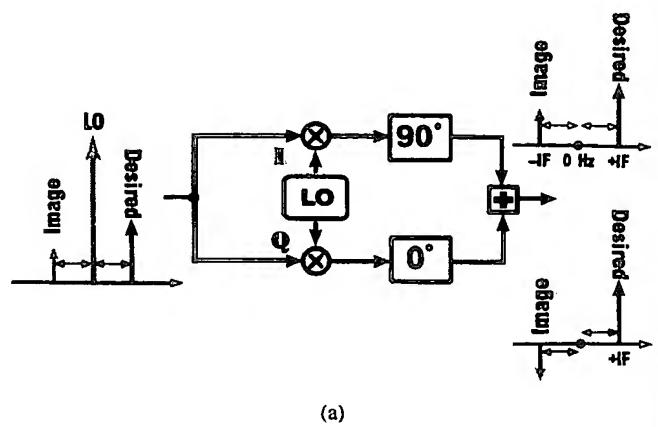
Fig. 1. Frequency plan of a superheterodyne receiver. Choice of IF is governed by width of preselect filter passband. The RF preselect and IF filters work together to select the desired channel.

In a standard broadcast FM receiver, for instance, the 10.7 MHz IF guarantees that the image channel lies outside the 20 MHz wide FM band. Therefore, even if the preselect filter inadequately suppresses the image, which is assumed not to be an FM signal, the subsequent frequency-discriminating detector will inherently tend to reject it. This relaxes the selectivity of the 100 MHz preselect filter, which may be constructed with either a single or ganged collection of *LC*-tuned circuits. Ceramic filters are an enabling technology for the 10.7 MHz FM IF. These small and cheap filters

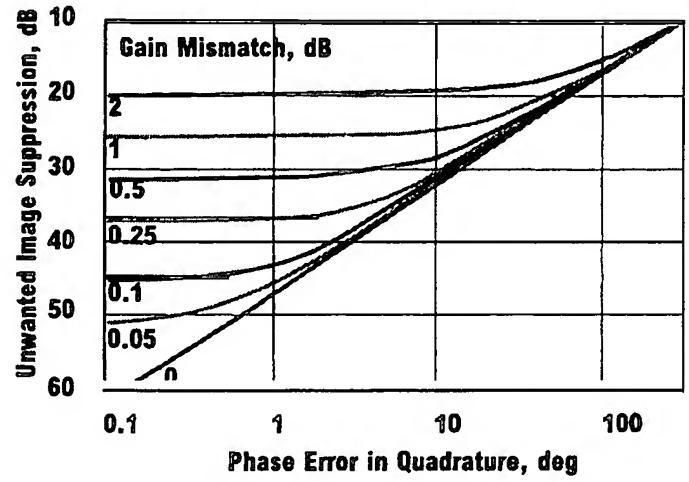
offer a narrow passband and good stopband attenuation, and they are widely used. The traditional 43.5 MHz IF in a TV receiver cannot suppress the image across the entire VHF, hyperband, and UHF bands, so as the receiver is tuned across various sub-bands, one of an array of RF narrowband filters is switched into the RF front-end [3] to suppress the image channel. Many analog cellular telephones use a 90 MHz IF. Amplification and filtering at these high intermediate frequencies between 10–100 MHz comes at the price of power dissipation because transistors must be biased at large currents to drive the parasitic and the low characteristic impedance of the passive IF filters. Further, the IF strip may require a large number of *off-chip passive* components, which add to receiver size. Although these are not serious problems for tabletop receivers—the easy alignment of a superheterodyne, resulting in a high selectivity, was always one of its strengths—they may become limitations in miniature, low power transceivers.

Wireless receivers must often handle very weak channels existing side-by-side with very strong channels in the same band. Thus, in addition to a minimum *stopband attenuation* to suppress the image channel, the filter must also have a wide *dynamic range*, that is, the ability to handle strong signals without distortion while remaining sensitive to weak signals above the intrinsic noise level in the passband. In this respect, passive filters are almost always superior, as the small-signal handling of active bandpass filters is limited by a fundamentally higher noise level [4], and nonlinearity in the active device tends to distort large signals. The dynamic range of active filters may only be increased at the expense of capacitor size and power dissipation.

Although most often a passive RF preselect filter attenuates the image channel, it may also be suppressed by selective *signal cancellation*. Here, the entire RF spectrum is downconverted to an IF in two identical mixers driven by quadrature phases of a local oscillator (LO). The downconverted spectra in the two branches are subjected to a 90° phase-shift relative to one another and then added (Fig. 2(a)). With appropriate design, this arrangement downconverts the desired channel to IF with the same phase in the two branches and the image channel to $-IF$ but antiphase in the two branches. After addition, the desired channel appears at the output with double strength, while the image channel subtracts and disappears. This *image-reject downconverter* is the dual of Weaver's celebrated phasing method of sideband selection [5], which is discussed later in the section on transmitters. In practice, departures from quadrature in the two LO signals and gain mismatch in the two branches will limit the extent of signal cancellation (Fig. 2(b)). When used in a receiver, the effectiveness of this image-suppression method is further limited by the wide dynamic range of radio signals. If the unwanted image channel is much stronger than the desired one, then after imperfect signal cancellation, it may only be suppressed to a comparable level to the desired channel, resulting in an intolerably large interference. Nevertheless, this type of downconverter is used, for instance, in a single-chip broadcast FM receiver with a low IF of 150 kHz [6].



(a)



(b)

Fig. 2. (a) The image-canceling downconversion mixer. The desired signal appears in-phase in the two branches and the undesired signal anti-phase. Allpass filters may be used to synthesize 90° phase shift. (b) Unwanted signal suppression as a function of errors in phase from ideal quadrature, with gain mismatch in the two branches as a parameter,

II. THE DIRECT-CONVERSION ARCHITECTURE

Suppose that the IF in a superheterodyne is reduced to zero. The LO will then translate the center of the desired channel to 0 Hz, and the portion of the channel translated to the negative frequency half-axis becomes the image to the other half of the *same* channel translated to the positive frequency half-axis (Fig. 3). The downconverted signal must be reconstituted by a phasing method of the type described above, otherwise the negative-frequency half-channel will fold over and superpose on to the positive-frequency half-channel. Zero-IF, therefore, mandates quadrature downconversion into two arms and a vector-detection scheme. However, this scheme does not suffer from the strong-image problem when the image-reject downconverter is used in a nonzero IF heterodyne receiver, and the typical gain mismatches and phase errors in the two branches cause only a small loss in detected SNR. A lowpass filter, which is in effect a bandpass centered at dc when the negative frequency axis is included, may be used to select the desired channel and to reject all adjacent channels. Therefore, RF preselection may in principle be

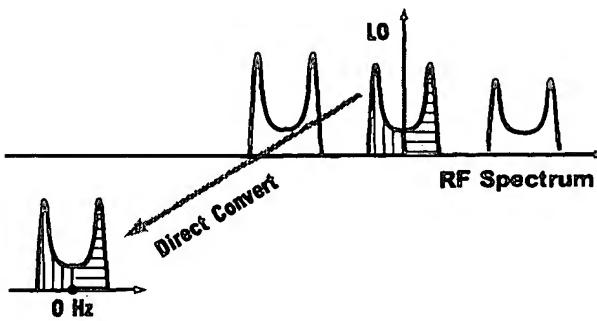


Fig. 3. Spectrum before and after direct-conversion

eliminated because there is no image channel. In practice, it is still required to suppress strong out-of-band signals that may create large intermodulation distortion in the front-end prior to baseband channel selection and to avoid harmonic downconversion. There is also the advantage that if a high-order active filter is used for channel selection, it will dissipate lower power and occupy a smaller chip area at a given dynamic range than an active bandpass filter with the same selectivity centered at a high IF [4]. All amplification past the front-end is also at baseband, and therefore consumes a small power. This zero-IF scheme is also called *direct-conversion*. When the local oscillator is synchronized in phase with the incoming carrier frequency, the receiver is called a *homodyne*.

As early as 1924, radio pioneers had considered use of homodyne architectures for single vacuum-tube receivers, but it was a homodyne measuring instrument for carrier-based telephony built in 1947 that first employed a high-order lowpass filter for channel-selection [7]. Thereafter, the concept lay dormant, until it was revived in 1980 in the radio-paging receiver, the first miniature digital wireless device for personal communication to attain widespread consumer use.

III. DIRECT-CONVERSION FSK RECEIVERS

Digital data in broadcast paging modulates the carrier by frequency-shift keying (FSK). The carrier frequencies may lie in the 400 MHz or the 900 MHz bands and binary data at 512 b/s or 1.2 kb/s rates shifts the carrier frequency by ± 4.5 kHz. This large modulation index results in a spectrum with two lobes symmetrically offset around the carrier (Fig. 3). Vance at ITT Standard Telecommunications Labs was the first to apply direct-conversion to this signal spectrum with a *single-chip* paging receiver [8], thus establishing a key concept for small, light paging receivers. Not all pagers today, though, use direct-conversion; some continue to use the superheterodyne implementation for higher performance [9].

Following a single-stage of RF amplification in this simple FSK receiver (Fig. 4), a local oscillator (LO) tuned to the incoming carrier downconverts the center of the desired paging channel to dc. In fact, quadrature phases of the LO downconvert the signal into two branches, labeled I and Q, enabling the detector to discriminate the signal at positive and negative frequencies (i.e., data 1's and 0's). A high-order *lowpass filter* in each branch with a cut-off at about 10 kHz selects the

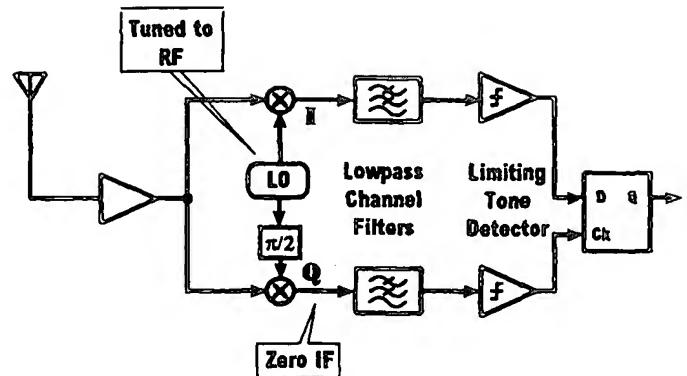


Fig. 4. Block diagram of a direct-conversion FSK receiver as may be used for radiopaging signals.

desired channel, while all other channels fall into the filter stopband. This may be integrated as a low-power active filter. A single-chip paging receiver from Philips uses a tenth-order continuous-time lowpass filter [10]. The data is encoded in the zero-crossings of the downconverted and filtered signal, which a limiter then amplifies to logic levels, eliminating the need for AGC. However, dc offsets directly add to the downconverted signal and may be so large as to disable zero-crossings in the limiter output, causing the receiver to fail to detect data. This problem is overcome by capacitively coupling the baseband signal path into the limiter to null these offsets. Some of the consequences of capacitive coupling are discussed in Section VI.

The detector is, in principle, only a flip-flop, driven at the D input by the I branch limiter and at the CK input by the Q branch limiter. The flip-flop output attains one steady-state if transitions at the CK input lead the transitions at the D-input and the other state if they lag. This corresponds exactly to a positive or negative frequency shift of the carrier, and thus, the data. Although this simple detector is found in many FSK receivers, it is susceptible to upset from a single noise impulse at the input. A more sophisticated detector oversamples the limiter output at a multiple of the data rate, thereby more finely quantizing the zero-crossing instant, and correlates this with quadrature phases of the expected frequency shift (4.5 kHz in the paging channel). The correlated output from the I and Q channels is integrated over a bit period, and the bit decision is made depending on which of the integrators first crosses a preset threshold. Correlation reduces the noise bandwidth. A one-bit implementation of this correlation detector in a spread-spectrum FSK receiver shows that it is very compact and dissipates a small power [11].

There are now many low-power, single-chip bipolar IC's implementing direct-conversion paging receivers [10], some operating at a supply as low as 1.1 V [12]. The on-chip capacitors required by the two active lowpass filters and ac coupling after downconversion occupy a large portion of the total die area. Aside from a reference crystal, the circuits only need some miniature off-chip inductors for the tuned RF amplifier loads and sometimes for the quadrature phase-shift network. The complete pager, including the microprocessor

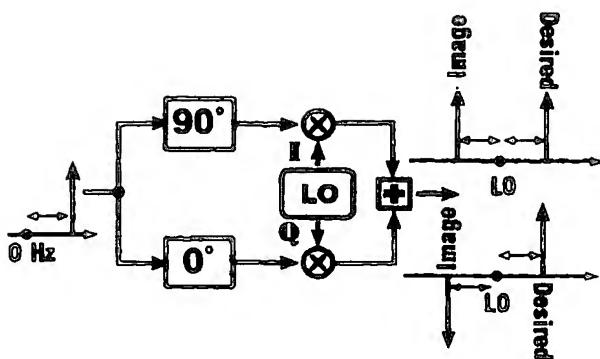


Fig. 5. A direct-upconversion mixer using the phasing method for selecting one sideband. Either one of the sidebands may be selected by combining the branches with the appropriate sign,

and display driver, may be a two-chip device with battery life in excess of six months.

One may appreciate the simplicity of a direct-conversion state-of-the-art paging receiver by comparing its inventory of parts with a superheterodyne implementation of the same built in a comparable technology [13]. The superheterodyne requires one more crystal, two trim capacitors, and a SAW filter, which together add a significant fraction to the total parts count, thus increasing the physical volume of the receiver and its power dissipation.

IV. DIRECT-CONVERSION SINGLE-SIDEBAND SYNTHESIZERS

For reasons of spectral efficiency, the transmitted signal in digital communications is usually single-sideband with suppressed-carrier. It would require an RF filter with a very sharp transition band to suppress one sideband on the modulated carrier while passing the other. The much more practical solution is the phasing method [5], where the modulated signal is first synthesized in quadrature at baseband, *directly-upconverted* into two branches by a quadrature LO centered at the carrier frequency, and added or subtracted to select either the upper or lower sideband (Fig. 5). The phasing method of sideband selection has been used for many years in single-sideband communication transceivers.

The unwanted sideband is suppressed to an extent limited by the gain mismatch in the two upconversion branches and by departures from quadrature in the two LO outputs (Fig. 2(b)). The dc offsets in the branches produce an output tone at the LO frequency. The unwanted sideband and LO leakage are unavoidable spurious emissions in the transmitted spectrum. Although the two upconversion branches will match well on the same IC, a gain mismatch as small as 1% (0.1 dB) limits unwanted sideband suppression to about 45 dB. With this gain mismatch, a phase-error of up to 1° is tolerable between the two LO outputs before the unwanted sideband grows further in relative amplitude. These mismatches may be trimmed at time of transceiver manufacture or self-calibrated with loopback modes that are activated during idle times to sense and suppress the unwanted sideband. Some trimming and adaptive methods are discussed in Section VII.

As the LO frequency in a direct-upconverter is centered in the transmit band, energy at this frequency may be spuriously radiated through parasitic unbalanced coupling into the power amplifier or antenna. For instance, the single-ended signal produced by an on-chip oscillator circuit tuned with an off-chip resonator may couple to the power amplifier input across pins of the RF package. Frequency-offset multi-step upconversion schemes, which are the dual of a heterodyne downconverter have been proposed [14] to combat this coupling problem. However, as LO phase-noise in a transmitter appears as noise added to the emitted signal, a process called *reciprocal mixing* in the radio literature, direct upconversion has the advantage over a frequency-offset scheme that only *one* LO contributes noise. Other spurious output tones in a single-sideband transmitter may arise from parasitic remixing of the modulated output with the baseband signal and by intermodulation distortion in the output stage [15]. Balanced circuit topologies on-chip LO's that require no external resonators [1], [16], and the lowered transmit power levels required in microcells, are all expected to lessen the magnitude of these problems.

V. DIRECT-CONVERSION RECEIVERS FOR DIGITAL CELLULAR TELEPHONES

Designers of portable digital cellular telephones are very interested in low-power radio architectures. Several integrated receiver and transmitter IC's conforming to established standards such as GSM and DECT have been developed in the past few years. This section summarizes some of their main features.

All transmitters in these portable phones use direct upconversion to produce a single-sideband output. In receivers, however, the superheterodyne architecture is more common. For instance, a 900 MHz bipolar IC GSM receiver from Siemens [17] downconverts the amplified RF signal from an off-chip low-noise amplifier to an IF of 45–90 MHz (Fig. 6). At this IF, the image lies in the stopband of the fixed RF preselect SAW filter. The amplified IF signal is sent to another off-chip SAW filter to reject adjacent channels. A quadrature mixer then downconverts the signal to baseband, and the vector baseband signal is finally detected. This architecture is preserved in later generations of this transceiver operating up to 2 GHz for DECT use [18], [19]. Other recent GSM transceivers build on a similar single superheterodyne architecture [20], in one case with a very high IF of 400 MHz [21]. Alcatel has publicized its use of direct-conversion in GSM and DECT receivers [22]–[24], although others [25] are exploring its possible use, and not all companies using direct conversion have published their experience. Alcatel's RF front-end is a relatively small silicon bipolar IC (Fig. 7), and the remainder of the signal processing, including lowpass channel-select filtering, takes place at baseband in a mixed analog-digital CMOS IC [26].

Given the many decades of familiarity with the superheterodyne, there will likely remain some reluctance towards adopting a new architecture until there is widespread experience in its effectiveness. However, direct-conversion also suffers from some unique problems to which the superheterodyne is immune. These are discussed in the following section.

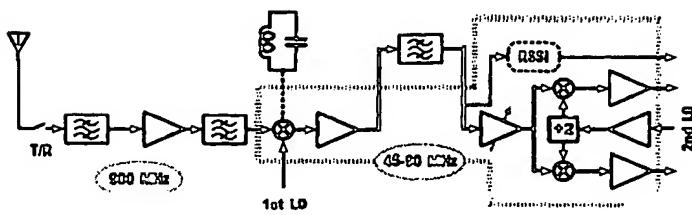


Fig. 6. A superheterodyne receiver for a digital cellular telephone.

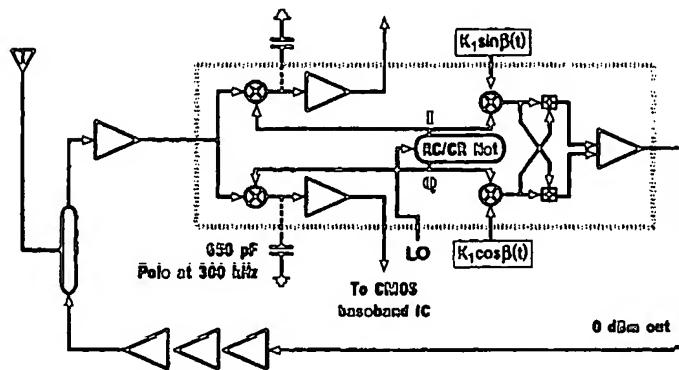
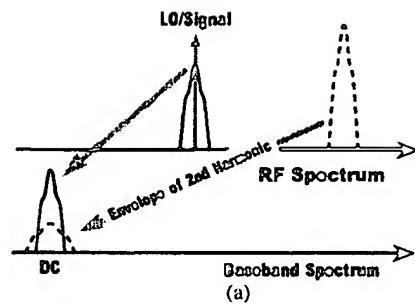


Fig. 7. A direct-conversion receiver and transmitter for a digital cellular telephone.

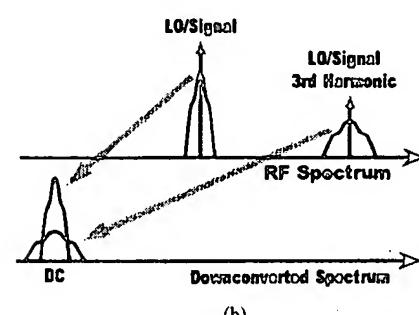
VI. PROBLEMS IN DIRECT-CONVERSION RECEIVERS

Among the problems in direct-conversion receivers, spurious *LO leakage* is probably best known. This arises because the LO in a direct-conversion receiver is tuned exactly to the center of the LNA and antenna passbands. In receive mode, a small fraction of the LO energy may make its way back to the antenna through the mixer and LNA, owing to their finite reverse isolation, or couple into the antenna through external leads, and then radiate out [27]. This becomes an in-band interferer to other nearby receivers tuned to the same band, and for some of them it may even be stronger than the desired signal. Regulatory bodies such as the FCC strictly limit the magnitude of this type of spurious LO emission. The problem is much less severe in a superheterodyne whose LO frequency usually lies outside the antenna passband. However, experimental studies [28] suggest that standard shielding in the receiver may control LO leakage to the point that it does not seriously handicap the use of direct-conversion.

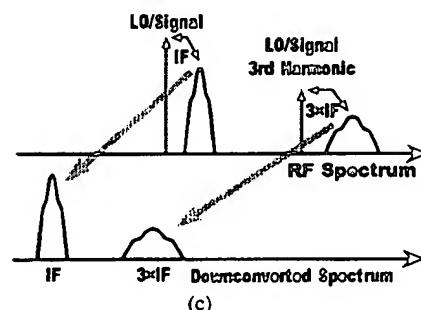
Distortion produced by strong signals in the downconversion mixer will cause the sensitivity of a direct-conversion receiver to degrade more rapidly than of the superheterodyne. Second-order distortion in a single-ended mixer will rectify the envelope of an amplitude-modulated RF input such as QPSK data to produce spurious baseband spectral energy centered at dc, which then adds to the desired downconverted signal [25], [27] (Fig. 8(a)). This is particularly serious if the envelope is that of a large unwanted signal lying in the preselect filter passband, which has not yet been rejected by the baseband channel-select filter. The most effective solution is to use



(a)



(b)



(c)

Fig. 8. Spurious downconversion caused by nonlinearity in a direct-conversion receiver. (a) Second-order distortion detects envelope of near-band interferer at baseband, overlaying desired signal, (b) LO harmonics downconvert signal harmonics to baseband, resulting in interference, (c) whereas in a superheterodyne downconverted harmonic products lie in IF stopband.

balanced circuits in the RF front-end, particularly the mixer, which will only create odd-order distortion.

However, even in a balanced circuit, the third harmonic of the desired signal may downconvert the third LO overtone to create spurious dc energy competing with the fundamental downconverted signal (Fig. 8(b)), whereas in a superheterodyne this downconverted component lies in the stopband of the IF filter (Fig. 8(c)). This is a small effect to the extent

¹There is no fundamental loss of noise figure in a balanced front-end. When the antenna signal drives a balanced low-noise amplifier through a power-splitting balun, the noise figure is exactly the same as directly driving the signal into a single-ended half circuit. However, the balanced circuit drains twice the current of the single-ended half circuit.

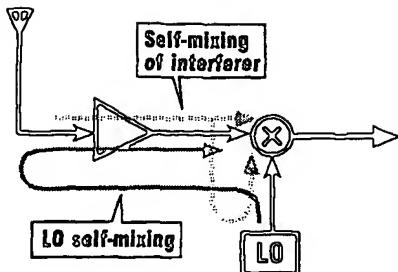
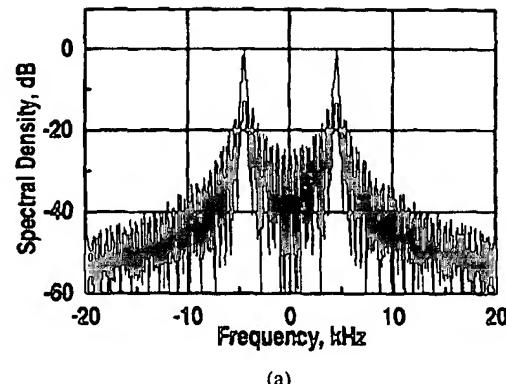


Fig. 9. Some sources of dynamic offset in a direct-conversion receiver. The LO may leak into the antenna, reflect off external objects, and downconvert to dc. A strong interferer may leak into the LO port and downconvert itself to dc. These dc offsets vary with physical location.

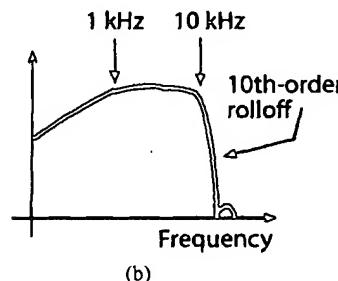
that both are third-order terms. To suppress this harmonic downconversion, mixers with embedded overtone-rejection bandpass filters have been proposed [29]. If exactly the same immunity to spurious downconversion is sought as in a superheterodyne, the direct-conversion receiver must use a balanced mixer with inherently greater linearity. Again, this is not an insurmountable obstacle; mixer linearity and related design issues are discussed in Section VII.

Perhaps the most serious problem is that of dc offset in the baseband section of the receiver following the mixer. This offset appears in the middle of the downconverted signal spectrum, and may be larger than the signal itself, and much larger than thermal and flicker noise. For instance, a downconverted signal of a few hundreds of microvolt rms may compete with an offset of a few millivolts. Unless the offset is removed, the SNR at the detector input will be very low. Offset arises, first, from transistor mismatch in the signal path between the mixer and the I and Q inputs to the detector. To this will add other offsets peculiar to the wireless environment [24], [30]. As described above, the LO signal leaking from the antenna during receive mode may reflect off an external object and self-downconvert to dc in the mixer (Fig. 9). Similarly, a large undesired near-channel interferer in the preselect filter passband may leak into the LO port of the mixer and self-downconvert to dc. These offsets are insidious because their magnitude changes with receiver location and orientation, and in a frequency-hopping receiver, with the instantaneous LO frequency. It is unlikely whether through better circuit design alone, the reverse isolation of mixers and LNA's can be improved to the point that these offsets become on the order of thermal noise. Appropriate circuits must be built into the receiver to remove them.

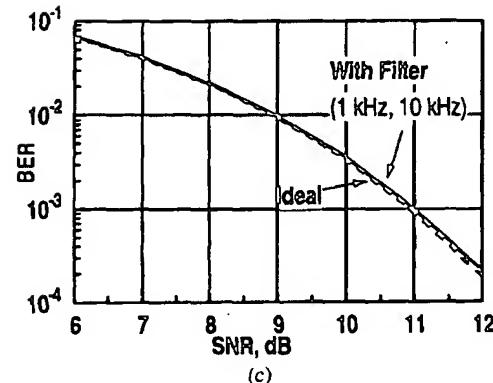
In the direct-conversion paging receiver, dc offset is removed by *capacitively coupling* the baseband circuits up to, and including, the limiter. Owing to the high impedance levels of active filters, the coupling capacitors are small enough to be integrated on to the receiver IC [10], [31]. However, this simple solution only works because of the specific spectral features of wideband-FSK modulation [10]. The paging spectrum peaks at ± 4.5 kHz and dips at dc by at least 25 dB relative to its level at the peaks (Fig. 10(a)). Simulations show that a first-order capacitive coupling, which produces a lower cutoff at 1 kHz in the channel-select filter preceding the limiting amplifier (Fig. 10(b)), causes no loss



(a)



(b)

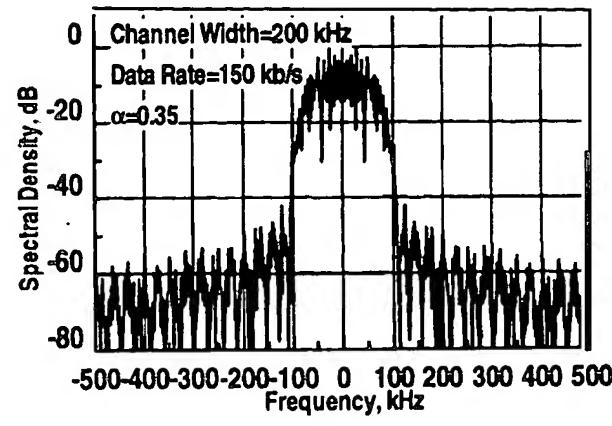


(c)

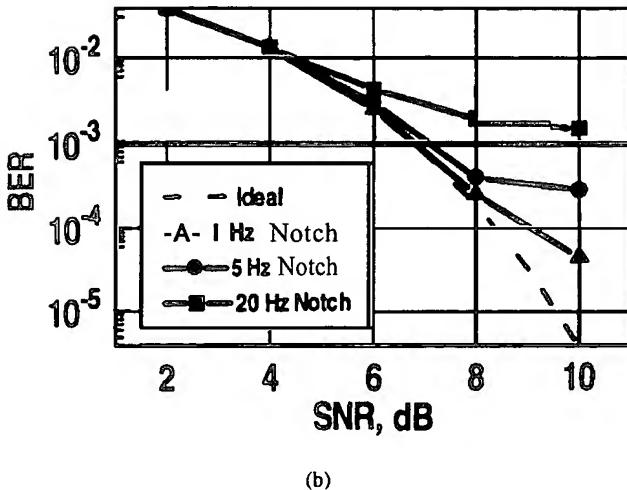
Fig. 10. (a) Downconverted spectrum of a paging channel carrying 500 b/s with 4.5 kHz carrier frequency keying. (b) A typical channel-select filter in the receiver, with a 1 kHz lower cutoff frequency to null dc offsets. Channels are spaced apart by 25 kHz. (c) Receiver sensitivity simulation, comparing an ideal offset-free receiver containing 10 kHz brickwall filter, with receiver suffering from offset, but using the filter in (b).

in receiver sensitivity (Fig. 10(c)) when the channel filter captures the valuable signal spectrum between 1–10 kHz. These are precisely the characteristics of the channel-select filter in a Philips single-chip paging receiver [10].

A small *frequency-error* between the transmitter and receiver LO's will cause the signal to downconvert asymmetrically around dc, and the capacitively-coupled filter may now place its notch in one of the two signal-bearing spectral lobes. For instance, a 5 ppm relative frequency-error at 900 MHz places the capacitive notch 4.5 kHz away from the center of the spectrum in the middle of one of the lobes. This limits the acceptable frequency tolerance on the crystal



(a)



(b)

Fig. 11. (a) Typical direct downconverted spectrum of an efficiently modulated carrier, here a cosine-filtered BPSK. (b) The impact of a notch of varying widths at dc on receiver performance. At speech-quality BER of 10^{-3} , the receiver ceases to function if the notch width is 20 Hz.

oscillator regulating the LO. In the absence of a sufficiently stable frequency reference, some form of automatic frequency-control must be used. The LO frequency error may be deduced from the long-term average of the frequency shifts keyed by pseudorandom data, which should ideally be zero after downconversion. This may be used as a correction signal on a varactor diode, or equivalent means of fine-tuning the LO. In a mostly digital implementation of a frequency-hopped FSK receiver, a numerically-controlled oscillator with resolution of a few hertz compensates frequency errors in the receiver clock as part of a frequency-acquisition loop [32].

Wideband FSK is spectrally inefficient, but it is used in paging because of the very low data rates and small duty cycle of use. However, digital cellular systems must fit continuous voiceband traffic at 200–1100 kb/s into 50–100 kHz wide channels, and to do so they use other spectrally-efficient modulation schemes. The GSM system, for instance, employs Gaussian-Filtered Minimum-Shift Keying (GMSK), a sort of optimized FSK. Other systems may use single-ended or differential Quadrature Phase-Shift Keying (QPSK). The spectra of all these modulation schemes peak at dc (Fig. 11(a)).

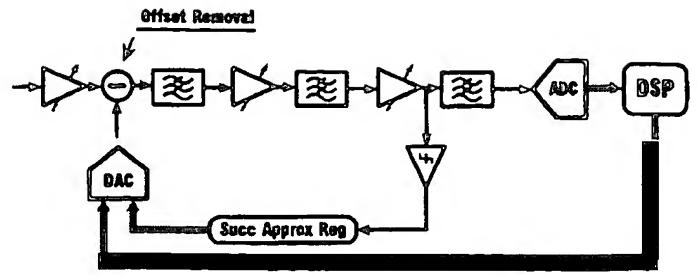


Fig. 12. Digital offset removal in a direct-conversion receiver. Offset is estimated from long-term average of digitized signal and subtracted from analog signal.

Following downconversion of the received signal to zero-IF, offsets will now directly add to the *peak* of the spectrum. It is no longer practical to null the offsets by capacitive coupling of the baseband signal path because signal energy will almost surely be lost from the spectral peak. Simulations on a representative 200 kHz wide spectrum (Fig. 11(b)) suggest that at a target bit-error rate of 10^{-3} , a 5 Hz notch at dc causes about 0.2 dB loss in receiver sensitivity, yet this notch need only widen to 20 Hz when the receiver will cease to function. It would require impractically large capacitors to produce this narrow notch, and the phase-distortion due to the *CR* coupling, which these simulations do not model, would cause the receiver performance to further deteriorate. Furthermore, during burst-mode communications, the capacitor would produce intolerably long transients.

DC offsets may be estimated and removed digitally [33], an approach Alcatel takes in their GSM receiver [26] (Fig. 12). The baseband signal is digitized and averaged in an 8-b DSP over a programmable time window. In addition, a 10-b successive-approximation A/D converter measures the analog signal polarity. These measurements are weighted together in a DAC, which subtracts off an estimate of the offset from the baseband signal. The spectrum loss around dc is only a few hertz, and digital filtering does not distort the group delay. The bandwidth of the feedback loop must be wide enough to accommodate the dynamic offsets described above. The settling time of the offset subtraction circuit may still cause loss of the first few symbols in a TDMA [30] or a frequency-hopping CDMA receiver.

Finally, when offsets have been satisfactorily nulled, flicker noise at the mixer output adds to the baseband signal. The SNR is lower than in a high-IF superheterodyne where only thermal noise is present. A bipolar transistor front-end may be superior in this respect to an FET circuit, but it is also possible to use autozero or double-correlated sampling to suppress flicker noise in MOS opamp-based circuits.

VII. COMPONENTS OF DIRECT-CONVERSION TRANSCEIVERS

A. Carrier-Frequency Local Oscillators with Quadrature Outputs

Direct-conversion transmitters and receivers need a local oscillator with quadrature outputs for vector modulation and demodulation, respectively. Whereas in a superheterodyne

receiver, the signal is quadrature-downconverted by a low frequency second LO, the greater challenge in direct-conversion is to produce accurate quadrature phases with good amplitude match at the much higher *carrier-frequency*. An error in quadrature of less than 1° is usually desired. A conventional 900 MHz or 2 GHz oscillator tuned with a single *LC* circuit or an off-chip resonator only produces a single-phase output. Quadrature phases may then be derived by passing this through a phase-shift network, composed of an *RC* and a *CR* (Fig. 13(a)), which phase shifts by -45° and +45°, respectively. When the time constant is equal to the oscillation period, the amplitudes of the two phases are also the same. Inaccuracies in the actual values of *R* and *C* will lead to errors in quadrature and are compensated for by some form of on-chip trimming such as the addition of voltage-controlled correction vectors (Fig. 13(b)) [22], [23]. Other circuits to successively improve the quality of quadrature have been proposed [15], but the simplest of them all is the cascaded four-branch *RC* polyphase network [34] (Fig. 13(c)). This may be thought of as a generalized *RC-CR* network with a four-phase input and output. When driven at the input by four unequally spaced phasors, for instance only a single phase sinewave and its inverse, with the other two inputs grounded, the circuit reinforces one sequence of the four phases of oscillation, say clockwise, and attenuates the other counterclockwise sequence [35]. With quite mild tolerances on its components, it is possible to derive quadrature phases from this network with order-of-magnitude improvements in phase accuracy over the *RC-CR* network. The polyphase *RC* network has been recently used in this way in a monolithic downconversion mixer [36] to attain effectively a 0.5° phase error and 0.5 dB amplitude error. The network is at its most powerful in suppressing the undesired sideband in a single-sideband upconverter, where it takes as its four inputs the balanced signals on the two mixer output branches (Fig. 5). Unwanted sideband suppression of as large as 60 dB has been reported [35].

Alternatively, quadrature phases are obtained at the outputs of positive- and negative-edge triggered flip-flops dividing a clock at *twice the carrier frequency* by two. In a direct upconversion IC for GSM where this scheme is used, output phase errors caused by unequal delays in the two flip-flops, and by departures from 50% duty cycle in the double-frequency oscillation, are found to be less than 1° [17] (Fig. 14). An on-chip bandpass filter improves duty cycle accuracy by suppressing harmonics of the double-frequency oscillation. However, the portions of the circuit operating at the double-frequency may become a speed bottleneck.

Quadrature outputs may also be tapped from a *polyphase oscillator*, such as a variable-frequency ring oscillator. In a four-delay stage ring oscillator, taps at diametrically-opposite points yield quadrature phases at every oscillation frequency [37] (Fig. 15). When the oscillator is composed of an odd-number of unit delays, the desired phases may be synthesized by interpolating two taps with a voltage-controlled phase-shifter in feedback around a quadrature-sensing circuit [38]. Mismatches in the delays of the unit cells limit the attainable phase accuracy. It is possible to keep phase errors to less than

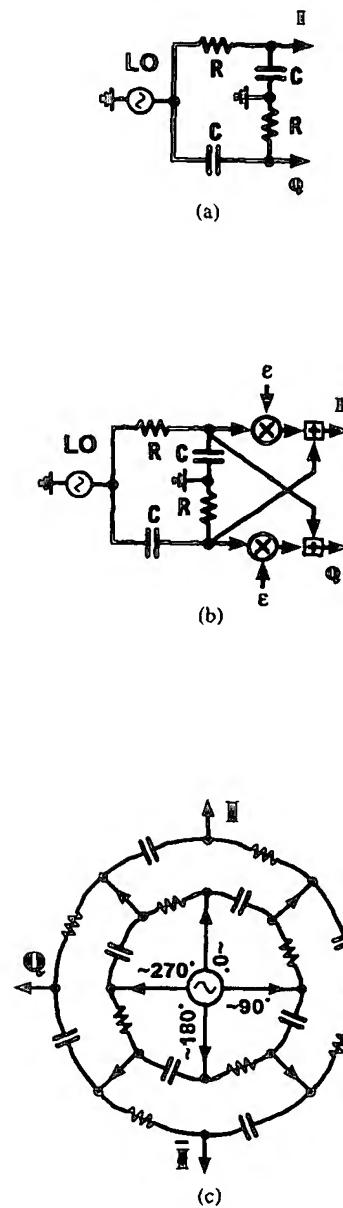


Fig. 13, Methods to derive quadrature phases from a single-phase oscillation
 (a) The *RC-CR* phase-shift network, whose accuracy depends on matching of *R*'s and *C*'s. (b) An extension to add programmable vector correction under voltage control. (c) Two stages in cascade of an *RC* polyphase network which may be driven at the input with only a single phase and its inverse, and which precisely produces four phases at the output even with lax component matching.

1° with careful balance of the capacitive loading on all the oscillator taps.

This form of resonator-less oscillator is attractive because it is fully integrable. It may be used when the specifications on phase-noise close to the carrier are not as stringent as they are, for instance, in analog cellular telephones [39], where the oscillator must use a passive, off-chip high-*Q* resonator. The free-running oscillator should obviously be designed for inherently low phase-noise, and for frequency stability it must also be slaved to a crystal reference in a frequency-locked loop. The loop gain and bandwidth should be chosen specifically to suppress phase-noise. The loop

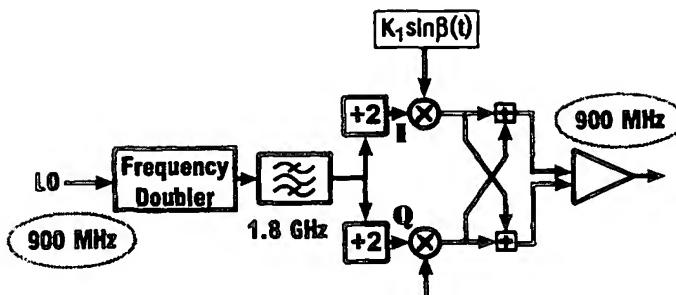


Fig. 14. A single-sideband upconversion circuit, where quadrature LO phases are derived by doubling LO frequency, and dividing down in $\div 2$ flip-flops triggered on opposite edges. Quadrature baseband modulated signal is digitally synthesized. Sideband selection in final differential RF amplifier.

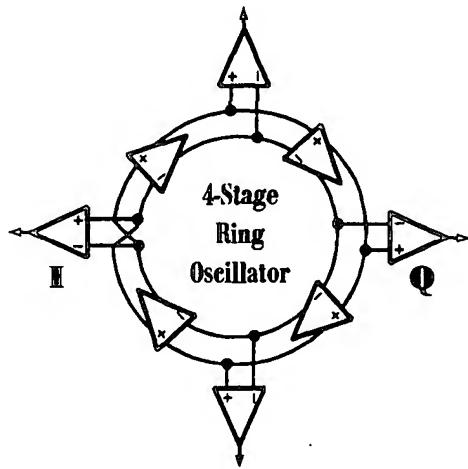


Fig. 15. A polyphase, voltage-controlled ring oscillator. The small number of delay stages lead to a high frequency of oscillation. Quadrature phases at diametrically opposite taps. This oscillator is readily integrable.

gain, which is infinite at dc because of the phase-integrating VCO, typically starts with a second-order frequency roll-off, and slows down to a first-order frequency roll-off prior to crossing unity gain [40]. Over the region of second-order roll-off close to the oscillation frequency, the loop is able to very effectively suppress phase noise caused by low-frequency ($1/f$) fluctuations in a FET oscillator. The unity-gain frequency of the loop is normally designed to be an order-of-magnitude lower than the reference frequency, which is derived, say, from a 20 MHz crystal oscillator. Thus, at a 100 kHz offset from the LO, the loop suppresses noise by 20 dB or so. Measurements on a three-stage 900 MHz CMOS voltage-controlled ring oscillator dissipating 20 mW show open-loop phase noise levels of -90 dBc/Hz at a 100 kHz offset from the carrier [41]. When the loop suppresses this further by 20 dB, the phase noise becomes comparable to the measured results at a 100 kHz offset in resonator-based oscillators for digital cellular use [20], [42].

Resonator-based oscillators, in which the off-resonance feedback loop gain to noise collapses at a rate proportional to the square of resonator Q , tend to convert less of a given voltage- or current-noise in the circuit into phase noise [49]. By

combining a recently developed technology to fabricate large-value spiral inductors on CMOS substrates [50] with a special cross-coupling technique between two identical LC oscillators [51], it is possible to automatically derive quadrature outputs from a fully integrated LC resonator-based oscillator with lower phase noise than in a ring oscillator. However, owing to its usually large series winding resistance the on-chip inductor is relatively low Q , and it is therefore difficult to obtain dramatic improvements over the phase noise in a ring oscillator. The same approach may be more useful with high- Q off-chip inductors. Unlike the ring oscillator, strong voltage control of an LC oscillator's frequency requires varactor diodes.

To compare phase-noise specifications on the LO in a direct-conversion receiver with that in a superheterodyne, note that with a modest IF, the frequencies of the two LO's will be about the same. Therefore, for the same amount of allowed reciprocal mixing, the phase-noise specifications on the direct-conversion receiver LO are not significantly more stringent than on the first LO in the superheterodyne.

As an alternative to the various analog circuit techniques described so far, digital LMS adaptive algorithms at baseband may sense and compensate for phase- and gain-errors in quadrature upconverters and downconverters [43]. These algorithms may be used in receivers where a modest- to high-resolution A/D converter precedes the baseband signal conditioning, as is the trend in many modern wireless devices. Other methods to sense and correct unknown gain- and phase-errors have also been proposed, such as downconversion with a three-phase LO [44].

B. Mixers for Direct-Conversion

As was described above, direct-conversion receivers need a more linear mixer to attain the same performance as a superheterodyne. Mixers commutate the amplified RF signal with the LO. In the often-used bipolar mixer based on the Gilbert analog multiplier, this is a current-mode commutation. The subcircuit responsible for RF voltage-to-current conversion prior to the commutator usually determines the overall mixer linearity. Resistive degeneration of the differential pair V-to-I converter [22] improves mixer linearity, and indeed, the available dynamic range², at the expense of a higher noise figure. MOSFETs, on the other hand, make more linear open-loop V-to-I converters at high frequencies, due to the cancellation of the dominant quadratic nonlinearity in a balanced configuration. They are also excellent switches. Recent MOSFET implementations [36], [45] of 1 GHz downconversion mixers prove that they have a very wide dynamic range. However, a continuous-time MOSFET mixer will add a considerable flicker noise to an input it has downconverted to zero IF, thereby degrading receiver noise figure. Any mixer commutating at the carrier frequency in a direct-conversion receiver is also likely to leak LO energy into the antenna because of imperfect reverse isolation.

²Dynamic range of a differential pair increases with degeneration because the voltage linearity improves roughly proportionally to the degeneration, while noise, voltage increases as the square-root.

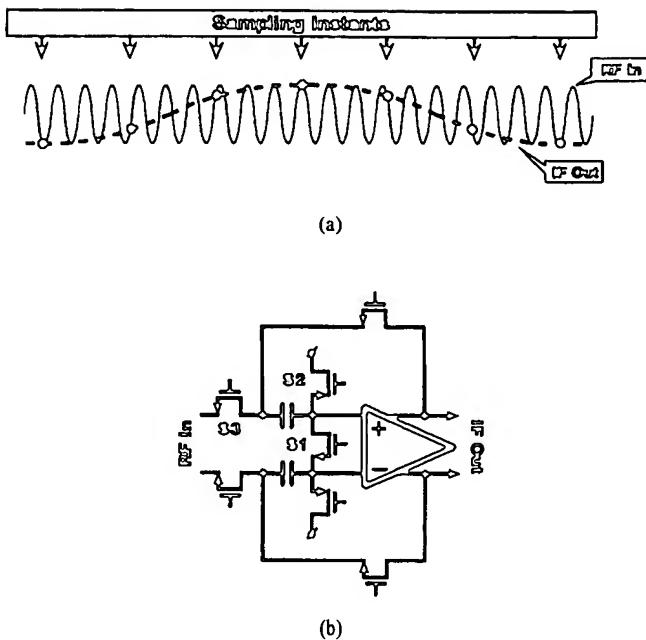


Fig. 16. (a) Downconversion by sampling a modulated RF carrier. A discrete-time (zero) IF signal is obtained when the sample rate is at least twice the modulation bandwidth and an integer divisor of RF carrier. (b) An implementation of the mixer. Switches S1 and S3, with the associated capacitors, form a wideband passive RF sampling network. Opamp is clocked at sample rate.

One way around these problems is to downconvert by *subsampling* the modulated RF [46] (Fig. 16(a)). The track-mode bandwidth of the sampling circuit must be greater than the input *carrier frequency*, whereas the (much lower) sampling rate must be at least twice the larger of the *modulation or spreading bandwidth* to downconvert without aliasing. The modulation appears at the output as a discrete-time beat between the RF input and sampling clock. Therefore, a sampling clock at an exact subharmonic of the input RF carrier accomplishes direct downconversion. The sampling clock is now the mixer's LO. Although one or more of the clock's high-order harmonics may leak into the LNA and antenna passband, any spurious radiation they produce is usually much weaker than due to an LO tuned to the carrier frequency.

The subsampling mixer tracks the input with a passive circuit consisting of FET switches and capacitors (Fig. 16(b)). The quadratic $I-V$ characteristic of MOSFET switches may contribute some distortion, but this is alleviated by a balanced implementation. The sampling clock is nominally a square wave with 50% duty cycle, whose falltime sets the switch sampling aperture. In a 1- μm CMOS implementation, the aperture may be as short as 200 ps [46]. The *non-zero* aperture in FET turn-off limits only the acquisition bandwidth but causes no distortion. However, *signal-dependent charge* injected from the nonlinear FET capacitances onto the sampling capacitor will distort the held signal. With the proper switching sequence, the injected charge is reduced by the opamp gain in hold mode [47]. The opamp is designed to clock at the sampling rate and to fully settle in hold mode.

An undesirable consequence of subsampling is that the circuit also tracks noise and possible interferers lying outside the Nyquist bandwidth (half the sample rate) and aliases these into the Nyquist bandwidth. Although adjacent channel interferers that are downconverted without aliasing will lie in the stopband of the subsequent channel-select filter, far-off interferers may alias into its passband and corrupt the desired signal. An RF preselect filter with a passband no wider than the Nyquist bandwidth of the mixer must be used at the antenna to attenuate these far-away interferers. Now, as sample rates as high as 100 MHz have been demonstrated in 1- μm CMOS op-amp circuits, a preselect filter centered at, say, 900 MHz may have up to a 50 MHz wide passband. Although this is not a highly selective filter, it must have a large stopband attenuation. The mixer still aliases broadband LNA output noise, which is bandlimited only by the low-Q tuned LNA load. A second preselect filter, identical to the first, when inserted between the LNA and mixer eliminates this aliasing, but this is not a desirable solution in a highly integrated receiver. In the absence of this second filter, then, the noise spectral density multiplied by aliasing competes with the downconverted signal and raises the receiver noise figure [46] to typically 6 dB or higher. The signal processing now required at the high clock frequency mixer input is not dissimilar to that in a high-IF superheterodyne. However, direct conversion still retains an advantage, in that after simple prefiltering, the mixer output may be decimated down to a lower clock at the channel-select filter. With some form of autozero during track mode, the input flicker noise in the opamp may be also suppressed. Owing to its wide dynamic range and low LO leakage, this may prove to be a useful mixer in direct-conversion receivers. As a secondary advantage, the discrete-time mixer output readily interfaces to a wide dynamic range, auto-zeroed switched-capacitor CMOS channel-select filter operating at a reduced clock rate.

VIII. CONCLUSIONS

The direct-conversion receiver eliminates many off-chip components and may offer significant power savings by amplifying a received signal mostly at dc rather than at an IF of tens or even hundreds of MHz. Direct-conversion is already widely used in single-sideband transmitters. Several problems in direct-conversion receivers have been identified, of which static and dynamic dc offset are probably the most important. In a wideband FSK receiver, this offset is removed very simply. Otherwise, DSP-based offset-removal must supplement good RF and baseband analog design in the receiver. Inspired by the simplicity of the paging receiver, our research group at UCLA is developing a single-chip spread-spectrum transceiver that uses binary-FSK modulation on a frequency-hopped carrier [48]. This transceiver uses direct-conversion in the transmit and receive paths.

With more practical experience, direct-conversion is expected to be used widely in certain wireless applications. This paper has summarized some of the key problems unique to direct-conversion and has presented various solutions. It is unlikely that a direct-conversion receiver that does not embody

some or all these solutions will ever be able to perform equally well with the superheterodyne. However, even with the added complexity of these solutions, the aggregate of direct conversion's advantages for a miniature, low-power radio transceiver is enough to warrant continued research and development.

ACKNOWLEDGMENT

The author is grateful to J. Sevenhans of Alcatel Bell Telephone for sharing his experience in direct-conversion receiver design and to J. Min of UCLA for the simulations underlying Figs. 10 and 11. Many graduate students at UCLA have contributed to some of the key RF-CMOS circuits described in this paper.

REFERENCES

- [1] A. A. Abidi, "Low-power radio-frequency IC's for portable communications," *Proc. IEEE*, vol. 83, no. 4, pp. 544-569, 1995.
- [2] L. Lessing, *Man of High Fidelity: Edwin Howard Armstrong, A Biography*. New York: Bantam Books, 1969.
- [3] S. Watanabe, *Semiconductor Devices for Electronic Tuners*, vol. 13. New York: Gordon and Breach, 1991.
- [4] A. A. Abidi, "Noise in active resonators and the available dynamic range," *IEEE Trans. Circuits Syst.*, vol. 39, no. 4, pp. 296-299, 1992.
- [5] D. K. Weaver, "A third method of generation and detection of single-sideband signals," *Proc. IRE*, vol. 44, no. 12, pp. 1703-1705, 1956.
- [6] T. Okanobu, H. Tomiyama, and H. Arimoto, "Advanced low-voltage single chip radio IC," *IEEE Trans. Consumer Electron.*, vol. 38, no. 3, pp. 465-475, 1992.
- [7] D. G. Tucker, "The history of the homodyne and synchrodyne," *J. British Inst. Radio Engineers*, vol. 14, no. 4, pp. 143-154, 1954.
- [8] I. A. W. Vance, "Fully integrated radio paging receiver," *IEE Proc.*, vol. 129, pt. F, no. 1, pp. 2-6, 1982.
- [9] K. Yamasaki, M. Matai, M. Miyashita, K. Yonekura, M. Inagaki, and Y. Morita, "Credit card size numeric display pager with microstrip antenna for 900 MHz band," in *NEC Research & Development*, vol. 34, no. 1, pp. 84-95, Jan. 1993.
- [10] J. F. Wilson, R. Youell, T. H. Richards, G. Luff, and R. Pilaski, "A single-chip VHF and UHF receiver for radio paging," *IEEE J. Solid-State Circuits*, vol. 26, no. 12, pp. 1944-1950, 1991.
- [11] J. Min, H.-C. Liu, A. Rofougaran, S. Khorram, H. Samueli, and A. A. Abidi, "Low power correlation detector for binary FSK direct-conversion receivers," *Electron. Lett.*, vol. 3, no. 13, pp. 1030-1032, 1995.
- [12] S. Tanaka, A. Nakajima, J. Nakagawa, A. Nakagoshi, and Y. Komianami, "High-frequency, low-voltage circuit technology for VHF paging receiver," *IEICE Trans. Fundamentals of Electron., Commun., Comput. Sci.*, vol. E76-A, no. 2, pp. 156-163, 1993.
- [13] K. Yamasaki, S. Yoshizawa, Y. Minami, T. Asai, Y. Nakano, and M. Kuroda, "Compact size numeric display pager with new receiving system," in *NEC Research & Development*, vol. 33, no. 1, pp. 73-81, Jan. 1992.
- [14] K. Negus, B. Koupal, J. Wholey, K. Carter, D. Millicker, C. Snapp, and N. Marion, "Highly integrated transmitter RFIC with monolithic narrowband tuning for digital cellular handsets," presented at *Int. Solid-State Circuits Conf.*, San Francisco, CA, 1994, pp. 38-39.
- [15] I. A. Koullias, J. H. Havens, I. G. Post, and P. E. Bronner, "A 900 MHz transceiver chip set for dual-mode cellular radio terminals," presented at *Int. Solid-State Circuits Conf.*, San Francisco, CA, 1993, pp. 140-141.
- [16] A. A. Abidi, "Radio-frequency integrated circuits for portable communications," presented at *Custom IC Conf.*, San Diego, CA, 1994, pp. 151-158.
- [17] J. Fenk, W. Birth, R. G. Irvine, P. Sehrig, and K. R. Schon, "An RF front-end for digital mobile radio," presented at *Bipolar Circuits and Technol. Meet.*, Minneapolis, MN, 1990, pp. 244-247.
- [18] V. Thomas, J. Fenk, and S. Beyer, "A one-chip 2 GHz single superhet receiver for 2 Mb/s FSK radio communication," presented at *Int. Solid-State Circuits Conf.*, San Francisco, CA, 1994, pp. 42-43.
- [19] W. Veit, J. Fenk, S. Ganser, K. Hadjizada, S. Heinen, H. Herrmann, and P. Sehrig, "A 2.7 V 800 MHz-2.1 GHz transceiver chipset for mobile radio applications in 25 GHz f, si-bipolar," presented at *Bipolar Circuits & Technol. Meet.*, Minneapolis, MN, 1994, pp. 175-178.
- [20] T. Stetzler, I. Post, J. Havens, and M. Koyama, "A 2.7-4.5 V single-chip GSM transceiver RF integrated circuit," presented at *Int. Solid-State Circuits Conf.*, San Francisco, CA, 1995, pp. 150-151.
- [21] C. Marshall, F. Behbahani, W. Birth, A. Fotowat, T. Fuchs, R. Gaethke, E. Heimerl, S. Lee, P. Moore, S. Navid, and E. Saur, "A 2.7 V GSM transceiver IC's with on-chip filtering," presented at *Int. Solid-State Circuits Conf.*, San Francisco, CA, 1995, pp. 148-149.
- [22] J. Sevenhans, A. Vanwesenae, J. Wenin, and J. Baro, "An integrated Si bipolar RF transceiver for a zero IF 900 MHz GSM digital radio front-end of a hand portable phone," presented at *Custom IC Conf.*, San Diego, CA, 1991, pp. 7.7/14.
- [23] J. Sevenhans, D. Haspeslagh, A. Delarbre, L. Kiss, Z. Chang, and J. F. Kukielka, "An analog radio front-end chip set for a 1.9 GHz mobile radio telephone application," presented at *Int. Solid-State Circuits Conf.*, San Francisco, CA, 1994, pp. 44-45.
- [24] J. Wenin, "IC's for digital cellular communication," presented at *European Solid-State Circuits Conf.*, Ulm, Germany, 1994, pp. 1-10.
- [25] C. Takahashi, R. Fujimoto, S. Arai, T. Itakura, T. Ueno, H. Tsurumi, H. Tanimoto, S. Watanabe, and K. Hirakawa, "A 1.9 GHz Si direct conversion receiver IC for QPSK modulation systems," presented at *Int. Solid-State Circuits Conf.*, San Francisco, CA, 1995, pp. 138-139.
- [26] D. Haspeslagh, J. Ceuterick, L. Kiss, and J. Wenin, "BBTRX: A baseband transceiver for a zero IF GSM hand portable station," presented at *Custom IC Conf.*, San Diego, CA, 1992, pp. 10.7.1-10.7.4.
- [27] N. C. Hamilton, "Aspects of direct conversion receiver design," presented at *Fifth Int. Conf HF Radio Syst. & Technol.*, Edinburgh, Scotland, 1991, pp. 299-303.
- [28] H. Tsurumi and T. Maeda, "Design study on a direct conversion receiver front-end for 280 MHz, 900 MHz, and 2.6 GHz band radio communication systems," presented at *IEEE Veh. Technol. Conf.*, St. Louis, MO, 1991, pp. 457-462.
- [29] J. M. Moniz and B. Maoz, "Improving the dynamic range of Si MMIC Gilbert cell mixers for homodyne receivers," presented at *Microwave & Millimeter- Wave Monolithic Circuits Symp.*, San Diego, CA, 1994, pp. 103-106.
- [30] G. Schultes, E. Bonek, A. L. Scholtz, and P. Kreuzgruber, "Low-cost direct conversion receiver structures for TDMA mobile communications," presented at *Sixth Int Conf Mobile Radio and Personal Commun.*, Coventry, UK, 1991, pp. 143-150.
- [31] A. Burt, "Direct conversion receivers come of age in the paging world," in *GEC Rev.*, vol. 7, no. 3, pp. 156-160, 1992.
- [32] H.-C. Liu, J. Min, and H. Samueli, "A low-power baseband receiver IC for frequency-hopped spread spectrum applications," presented at *Custom IC Conf.*, Santa Clara, CA, 1995, pp. 311-314.
- [33] A. Bateman and D. M. Haines, "Direct conversion transceiver design for compact low-cost portable mobile radio terminals," presented at *IEEE Veh. Technol. Conf.*, San Francisco, CA, 1989, pp. 57-62.
- [34] M. J. Gingell, "Single sideband modulation using sequence asymmetric polyphase networks," *Electrical Commun.*, vol. 48, no. 1-2, pp. 21-25, 1973.
- [35] R. C. V. Macario and I. D. Mejallie, "The phasing method for sideband selection in broadcast receivers," *EBU Rev. (Tech. Pt.)*, no. 181, pp. 119-125, 1980.
- [36] J. Crols and M. Steyaert, "A fully integrated 900 MHz CMOS double quadrature downconverter," presented at *Int. Solid-State Circuits Conf.*, San Francisco, CA, 1995, pp. 136-137.
- [37] A. W. Buchwald and K. W. Martin, "High-speed voltage-controlled oscillator with quadrature outputs," *Electron. Lett.*, vol. 27, no. 4, pp. 309-310, 1991.
- [38] S. K. Enam and A. A. Abidi, "NMOS IC'S for clock and data regeneration in Gb/s optical-fiber receivers," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1763-1774, 1992.
- [39] T. Uwano, T. Ishizaki, Y. Nakagawa, and T. Nakamura, "Design of a low-phase noise VCO for an analog cellular portable radio application," *Electron. & Commun. in Japan*, vol. 77, pt. 2, no. 3, pp. 58-65, 1994.
- [40] D. H. Wolaver, *Phase-Locked Loop Circuit Design*. Englewood Cliffs, NJ: Prentice-Hall, 1991.
- [41] M. Thamsiranunt and T. A. Kwasniewski, "CMOS VCO'S for PLL frequency synthesis in GHz digital mobile radio communications," presented at *Custom IC Conf.*, Santa Clara, CA, 1995, pp. 331-334.
- [42] S. Beyer and G. Lipperer, "Low-current oscillator design for 900 MHz GSM applications," in *Microwave Eng. Europe*, Oct. 1991, pp. 35-41.
- [43] J. K. Cavers and M. W. Liao, "Adaptive compensation for imbalance and offset losses in direct conversion transceivers," *IEEE Trans. Veh. Technol.*, vol. 42, no. 4, pp. 581-588, 1993.
- [44] R. K. Loper, "A tri-phase direct conversion receiver," presented at *Military Commun. Conf.*, Monterey, CA, 1990, pp. 1228-1232.

- [45] A. Rofougaran, J. Y.-C. Chang, M. Rofougaran, S. Khorram, and A. A. Abidi, "A 1 GHz CMOS RF front-end IC with wide dynamic range," in *European Solid-State Circuits Conf.*, Lille, France, 1995, pp. 250-253.
- [46] P. Y. Chan, A. Rofougaran, K. A. Ahmed, and A. A. Abidi, "A highly linear 1-GHz CMOS downconversion mixer," presented at *European Solid-State Circuits Conf.*, Sevilla, Spain, 1993, pp. 210-213.
- [47] Y.-M. Lin, B. Kim, and P. R. Gray, "A 13 b, 2.5 MHz self-calibrated pipelined A/D converter in 3- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 628-636, 1991.
- [48] J. Min, A. Rofougaran, H. Samueli, and A. A. Abidi, "An all-CMOS architecture for a low-power frequency-hopped 900 MHz spread-spectrum transceiver," presented at *Custom IC Conf.*, San Diego, CA, 1994, pp. 379-382.
- [49] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proc. IEEE*, vol. 54, no. 2, pp. 329-330, 1966.
- [50] J. Y.-C. Chang, A. A. Abidi, and M. Gaitan, "Large suspended inductors on silicon and their use in a 2- μ m CMOS RF amplifier," *IEEE Electron Device Lett.*, vol. 14, no. 5, pp. 246-248, 1993.
- [51] A. Rofougaran, J. J. Rael, M. Rofougaran, and A. A. Abidi, "A 900 MHz CMOS LC oscillator with quadrature outputs," to be presented at *Int. Solid-State Circuits Conf.*, San Francisco, CA, 1996.



Asad A. Abidi (S'75-M'80-SM'95) was born in 1956. He received the B. SC. (Hon.) degree from Imperial College, London in 1976 and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley in 1978 and 1981, respectively.

He was at Bell Laboratories, Murray Hill, NJ from 1981 to 1984 as a Member of the Technical Staff in the Advanced LSI Development Laboratory. Since 1985, he has been with the Electrical Engineering Department of the University of California,

Los Angeles where he is Professor. He was a Visiting Faculty Researcher at Hewlett Packard Laboratories during 1989. His research interests are in CMOS RF design, high-speed analog integrated circuit design, data conversion, and other techniques of analog signal processing.

Dr. Abidi served as the Program Secretary for the International Solid-State Circuits Conference from 1984 to 1990 and as General Chairman of the Symposium on VLSI Circuits in 1992. He was Secretary of the IEEE Solid-State Circuits Council from 1990 to 1991, and from 1992 to 1995, he was Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He received the 1988 TRW Award for Innovative Teaching.

REST AVAILABLE COPY